AMENDMENTS TO THE SPECIFICATION:

IN THE ABSTRACT:

Please replace the original page 51 with the accompanying replacement page 51, which includes the following rewritten paragraph beginning at page 51, line 2:

1 Encoder circuitry (39) for applying a low-density parity check (LDPC) code to 2 information words is disclosed. The encoder circuitry (39) takes advantage of a 3 macro matrix arrangement of the LDPC parity check matrix in which a left-hand 4 portion of the parity check matrix is arranged as an identity macro matrix, each 5 entry of the macro matrix corresponding to a permutation matrix having zero or 6 more circularly shifted diagonals. The encoder circuitry (39) includes a cyclic 7 multiply unit (88), which includes a circular shift unit (104) for shifting a portion of 8 the information word according to shift values stored in a shift value memory (82) 9 for the matrix entry, and a bitwise exclusive-OR function (106) for combining the 10 shifted entry with accumulated previous values for that matrix entry. Circuitry 11 (92, 96) for solving parity bits for row rank deficient portions of the parity check matrix is also included in the encoder circuitry (39). 12